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5 (A) applying a data bit from the data bitstream to each detecting element in a series of detecting elements, each detecting element in the series corresponding to a predetermined bit in the predetermined pattern;

(B) applying to each detecting element in the series of detecting elements the corresponding predetermined bit in the predetermined pattern of bits; and

10 (C) generating in each detecting element in the series of detecting elements an error signal indicative of the number of mismatches between the received data bit and the corresponding predetermined bit in the predetermined pattern in previous detecting elements in the series in previous clock cycles and in the current detecting element in the current clock cycle.

14. The method according to claim 13, further comprising the step of: receiving the data bitstream.

15. The method according to claim 13, further comprising the step of: applying an error signal from a previous detecting element in the series to each detecting element in the series of detecting elements.

16. The method according to claim 13, further comprising the step of: detecting that a predetermined maximum allowed number of mismatches has

been detected; and